PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-259499
(43)Date of publication of application : 22.09.2000

(51)Int.Cl. G06F 12/08

(21)Application number : 2000-019307
(22)Date of filing : 27.01.2000

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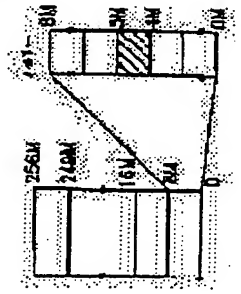
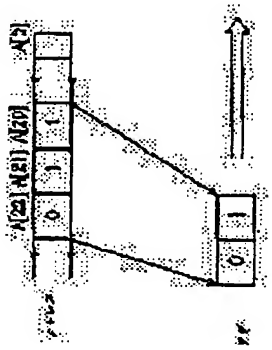
(30)Priority
Priority number : 99 88103217 Priority date : 03.03.1999 Priority country : TW

(54) METHOD FOR MAPPING DISTRIBUTING TYPE CACHE MEMORY

(57)Abstract:
PROBLEM TO BE SOLVED: To improve system efficiency by setting the uppermost and lowermost parts of a system memory where an operating system most frequently accesses to cache possible ranges.
SOLUTION: This mapping method selects a set of bits in an address bit string and uses it to correspond to a tag mapping table. The possible combinations of the values of selected specific bits make a system memory where the corresponding tag mapping table are mapped a cache possible area or a cache impossible area according to user definition. And the uppermost and lowermost layer parts of the system memory where access is frequency performed are simultaneously defined as cache possible parts. These areas can be defined as a cache possible area or a cache impossible area in accordance with user's needs. For this reason, the cache possible areas of the memory is not continuous distributions but necessary scattered distribution.





LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

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CLAIMS

[Claim(s)]
[Claim 1] The method of setting up the cache possible range of memory makes two or more bits of the address bit of a high order in an address bit string comparatively the bit dealing with a tag bit. When a bit is coded by the encoding method and the bit and tag bit after encoding are in agreement, Memory is the mapping method of the dispersion formula cache memory which is a cache possible portion, among those is characterized by setting beforehand the best layer and the lowest layer range of memory corresponding to these bits as the cache possible range.
[Claim 2] It is the mapping method of the dispersion formula cache memory characterized by memory being a cache possible portion when the method of setting up the cache possible range of memory makes two or more bits of the address bit of a high order in an address bit string comparatively the bit dealing with a tag bit, and codes a bit by the encoding method and the bit and tag bit after encoding are in agreement.
[Claim 3] The mapping method of the dispersion formula cache memory according to claim 2 characterized by setting up coincidence of the bit after encoding and a tag bit by the system.
[Claim 4] The mapping method of a dispersion formula cache memory according to claim 2 that the bit corresponding to memory is characterized by setting beforehand the range most frequently used by the system as the cache possible range.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Especially this invention relates to the mapping mode of a cache memory about the technology of the reading method of memory.
[0002]
[Description of the Prior Art] Drawing 1 is the block diagram of conventional cache memory equipment. Cache memory equipment 110 is mainly constituted by a cache memory 111 and the cache control circuit 112. The cache control circuit 112 controls a cache memory 111, and bears operation of the cache memory equipment 110 whole. A cache memory 111 contains reading storage 113 and the tag memory (tag RAM) 114 further. Reading storage (data RAM) 113 saves the data corresponding to system memory 140, and the tag memory 114 saves the address data corresponding to system memory 140. And it discriminates whether the bit was made into the dirty bit (dirty bit), and the data in reading storage 113 were updated.
[0003] Drawing 2 (A) shows a cache memory, system memory, and the correspondence situation of a between. Since only some data of system memory can be saved in a cache memory, the bit string corresponding to a part of address in the system memory of the data which saved the data corresponding to system memory in fact at reading storage, and reading storage saved is saved in tag memory. Therefore, what combined the index address of reading storage and the bit string in tag memory is equal to the actual address of system memory, as drawing 2 (B) shows. As for the address of each data in system memory, all cache memories have the address mapping of a position and data, this kind of cache memory structure is direct mapping (direct mapped), and the whole of each position of system memory is mapped by a certain position in a cache memory.
[0004] Some data of system memory can be saved in a cache memory, and it mainly writes to a cache memory at the time of CPU operation. therefore, a ******** [having surely hit the cache memory, when cache equipment processed the R/W data demand of CPU] -- or you have to judge whether the data of system memory are newly sent to memory The reading demand which CPU sent out, or when it writes and a demand is received, the judgment method of a hit compares the address of CPU sending out with the content of tag memory, and if the same, it will consider it as a hit. a cache memory -- the method of tag mapping -- memory -- a cache -- being possible (cachable) -- it sets up That is, this is the above-mentioned hit. There is a limitation in a general tag bit and, generally memory is divided into a cache possible portion and a cache impossible portion (non-cachable) in response to the influence which is a tag bit only for 8 bits or 7 bits.
[0005] If the case where the size of system memory has 256M by 512K, and a cache memory has a 8-bit tag temporarily is taken for an example, the maximum cache possible (cachable) range which can map it (mapping) will receive a limit of tag bit size. It is 28 times, 128M [i.e.,], the 512K, as drawing 3 shows. As the mapping method of the conventional cache memory makes the range of cache possible memory continue and part I part 200a of 256M system memory (system memory) of drawing 3 shows it, the range of 128M is a cache portion from 0M, and the memory of the range of 256M is set as the range of

impossible cache (non-cachable) memory by the cache possible controller (cachable controller) from 128M. it understands from having mentioned above -- as -- the tag mapping mode of the conventional cache memory -- memory -- simple -- two portions -- dividing -- a part -- lower layer cache possible memory 200a -- the part has already been divided into the upper cache impossible memory 200b Generally an operating system (operating system, OS) builds a stack (stack) or state maintenance (status keeping) using the upper memory, for example, starts a stack from the address of 256M from the address of 0M to a stack or above to down. Since only the lower layer portions 200a, 0-128M of memory were able to be made into the cache possible range by the tag mapping method of the conventional cache possible range, the efficiency of an operating system was very bad. Therefore, it was the technical problem of a cache memory how best layer 200b of system memory and lowest layer 200a are made into the cache possible range.

[0006]

[Problem(s) to be Solved by the Invention] Since the best layer part memory which an operating system accesses frequently since it has mapped by the tag mapping method of the conventional cache memory only to one continuous cache possible memory storage, i.e., the lower layer portion of system memory, was not able to be made into the cache memory possible range when it summarized having mentioned above, system-wide efficiency was bad.

[0007] The purpose of this invention is offering the mapping method of a dispersion formula cache memory, and using a part for a part for the best layer of system memory, and the lowest layer as the memory in which a cache's is possible. this invention -- a degree -- the purpose offers the mapping method of a dispersion formula cache memory, and abolishes the need of limiting to continuation memory storage, according to the need for cache possible range distribution of system memory The further purpose of this invention is offering the mapping method of a dispersion formula cache memory, setting a system memory portion with the most frequent access of an operating system as the cache possible range, and raising system efficiency.

[0008]

[Means for Solving the Problem] In order to attain the purposes of the above and other, if this invention offers the mapping method of a dispersion formula cache memory and describes it briefly, it will become as follows. The mapping method of the dispersion formula cache memory this specification printing chooses the address bit of a lot in an address bit string, and uses it for correspondence with a tag mapping table. By definition of a user, the possible combination of the value of the selected specific address bit makes system memory which the tag mapping table which carries out phase correspondence mapped a cache possible field or a cache impossible field. Because, since a user depends on adding and defining [a specific address bit] making into a cache possible field or a cache impossible field system memory which the tag mapping table mapped, a part for a part for the best layer of system memory and the lowest layer can be simultaneously defined as a cache portion. Or according to a demand of a user, these fields are made into the cache possible range or the cache impossible range, and the cache possible range of memory is considered as the distributed (scatter) distribution instead of continuous distribution doubled with the need.

[0009] By the mapping method which this invention submits, a user makes the best layer field and the lowest layer field of system memory which an operating system accesses frequently the cache possible range, and raises the efficiency of a system. In order to clarify more the above-mentioned purpose of this invention, the feature, and the advantage, a comparatively good operation gestalt is described below and detailed explanation is given together with a drawing.

[0010]

[Embodiments of the Invention] The mapping method of the dispersion formula cache memory of this invention uses as cache possible memory memory storage which a system accesses frequently, and raises the efficiency of system access memory. It is used for choosing the bit of the lot of the bit position of a high order comparatively, and corresponding with a tag mapping table (tag mapping table) in the bit string (address bit string) which shows the address. The possible combination of the value of the bit of a lot is

chosen, a user gives a definition, and system memory which the tag mapping table which carries out phase correspondence mapped is made into a cache possible field or a cache impossible field. A user adds a bit and a tag mapping table mapping and making system memory into a cache possible field or a cache impossible field gives a definition. Therefore, a part for a part for the best layer of system memory and the lowest layer can be simultaneously used as a cache possible portion. Or by a user's needs, the cache possible range of memory is considered as the distributed (scatter) distribution instead of continuous distribution by making those fields into the cache possible range or the cache impossible range.

[0011] Drawing 4 is the mapping method of the dispersion formula cache memory of this invention, shows a tag mapping table, memory, and the correspondence relation of a between, and explains the operation method and function of this invention. In an address bit string, the bit of the lot of the bit position of a high order is comparatively made into a tag bit and the corresponding address, and this bit passes through the encoding method. When the bit after encoding is in agreement with a tag bit, memory serves as a cache possible portion, makes the cache possible range of memory a dispersion formula by this, and does not carry out the type of the continuous distribution of the general former.

[0012] According to the example, it is made the bit which carries out phase correspondence of the bit [in an address bit string] A [22:20] with a tag, and the cache possible memory portion to which the tag mapping table by three bit combination corresponds is determined. Here, let what set memory capacity to 8M be an example. The size of the cache possible memory in which 512K maps a cache memory size and a tag maps a tag (tag) in the case of the number of three places is 23 times, i.e., the size of 4M, the 512K. 4M in the memory of this, 8M [i.e.,], are that a cache is possible.

[0013] The address bit sum totals of A [22:20] are eight kinds of different combination, for example, it corresponds to eight memory storage, such as eight portions of memory, 8M-7M, 7M-6M, --, 2M-1M, and 1M-0M, in order of (111) from drawing 4 showing (000), respectively. Memory is divided into eight division into equal parts with this operation gestalt.

[0014] Because, generally an operating system builds maintenance of a stack or a state using the upper memory. Therefore, since the memory of the field is accessed frequently, a part for a part for the best layer and the lowest layer is beforehand set as the cache possible range. The size of two portions of 8M-7M of drawing 4 , and 1M-0M is 2M. The remaining range of 2M can be set up according to needs. Finally, as shown in drawing, the cache possible range in memory presents a dispersion formula distribution, and sets the best layer with the most frequent system access, and the lowest layer (for example, two portions of 8M-7M, and 1M-0M) as a cache possible portion. Thus, the efficiency of system access memory is raised sharply.

[0015] A [22:20] is the situation of (011) and that drawing 5 shows sets a tag code to (01) through the encoding method. Moreover, the corresponding memory range is the correspondence view which are 5M-4M. For this reason, when a cache memory has 512K and has a 8-bit tag, the size of cache possible memory is 128M. By making 8M into one unit, according to the above-mentioned method, the selected address and the selected encoding method turn a tag bit to the memory cache possible range, distribute, use as cache possible memory the range which range systems, such as the memory upper layer and a lower layer portion, often use, and raise system efficiency.

[0016]

[Effect of the Invention] Therefore, the feature of this invention makes the specific bit in an address bit string the bit dealing with a tag bit, and when in agreement with a tag bit through the encoding method, this specific bit changes memory to a cache possible portion, makes the cache possible range of memory a dispersion formula, and considers it as a different type from the continuous distribution of the general former. Another feature of this invention is making a part for the best layer of system memory, and the lowest layer into the cache possible range. The efficiency of system access memory increases sharply by eye a partial hatchet with the access of an operating system most frequent [this portion], and this. Since the further feature of this invention can set up the cache possible range of system memory freely, it is not limited to the conventional continuous-distribution type.

[0017] although this invention was indicated according to the suitable operation gestalt, it is not for

limiting this invention from the first, and since [with natural correction] it is carried out and gets, if the range of the patent-right protection does not have a law in a suitable change row, in the range of the technical thought of this invention, it will not become it on the basis of a claim, and it and an equal field, so that clearly, if it becomes skilled in this technology

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TECHNICAL FIELD

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PRIOR ART

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EFFECT OF THE INVENTION

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